## REMARKS

This Amendment is responsive to the Office Action dated August 15, 1995, in the parent application. Claims 1-57 were pending and the Office Action rejected all claims. Claims 28-36 have been cancelled without prejudice. Claims 58-70 have been added. This Supplemental Preliminary Amendment supplements the Amendment filed on January 12, 1996 with the continuation request, and expands upon the claim amendments and arguments submitted therein.

The present invention relates to an improvement in program converting units (i.e. software compilers) and processors to run the output of the compiler. Specifically, the present invention is useful for "embedded" microprocessors which are used in a variety of commercial applications such as microwave ovens, dishwashers, automobiles, etc. The term "embedded" referring to the fact that the processor is physically embedded into the industrial device. In such commercial applications, using a general purpose microprocessor such as a Pentium CPU from Intel would not be cost effective since the control program may only use a fraction of the CPU's capacity. Therefore, there is a need for processors which have only the necessary capabilities to run a control program without any extra overhead. This results in an efficient use of memory and chip area and minimizes power consumption.

Since each product requires a different amount of programming to control its operation, the sizes of control programs can vary widely. Therefore, some applications may require a 16-bit address length in order to properly address the necessary memory. Other applications, however, may require a 19-bit address length in order to address the adequate amount of memory. In the 19-bit situation, the system designer could use a CPU with either a 24-bit or a 32-bit address length, but this would be wasteful. Thus, in the present invention a series of embedded microprocessors are created with N-bit length. The system designer can choose one of the processors to use for a given application with sufficient address length to address the required memory size for the control program.



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In order to compile the source control program under prior art systems, however, there would have to be a compiler written for each processor. As shown in Exhibit B (see previous Exhibit A in previous Amendment), prior art compilers are written such that the output machine language always has the same address length and data code length, no matter what the size of the input program. Thus, if the compiler is written for a 64-bit CPU, even a 20-line program will be compiled with a 64-bit address space. The output is thus "fixed" by the compiler. In the present invention, however, the programmer (i.e. user of the compiler) can designate as input to the compiler the desired address length N, and data length M, of the output machine language program. Thus, the output of the compiler varies with the user inputs. This is an improvement over prior art compilers in that this one compiler can then be used in conjunction with the series of processors to produce an embedded processor with associated control programming having a minimum size, resulting in cost-savings for the manufacturer.

Claims 1-5, 13-19, 44-46, 54, and 55 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants have amended the noted phrases "customized" and "both" and the claims should now satisfy 35 U.S.C. § 112. However, Applicants have not changed "a direction" or "a user's direction" as these are not indefinite, since a "direction" is an "instruction for doing, operating, using, preparing, etc." (Webster's New Universal Unabridged Dictionary). Applicants are using the words in the sense of this definition. Therefore, Claims 3 and 13 should satisfy 35 U.S.C. § 112, second paragraph.

Claims 1-5, 13-27, 44-57 were rejected under 35 U.S.C. § 103 as being unpatentable over Harmon in view of Sebesta and Killian et al. (U.S. Patent No. 5,420,992). The Office Action incorporated the rejection of the claims from the previous Office Action, and further provided Killian et al. to support the obviousness rejection. Applicants respectfully contend that Killian et al. does not teach "N being input by a user during an execution of the program converting unit, the value of N selected depending on the size of the source program," as claimed in amended Claim 1. Claims 1, 6, 11, 13, 20, and 27 all claim a user input. The reference cited by the Office Action, Col. 3, lines 33-55 of Killian et al. simply does not teach

any user input to a "program converting unit" (i.e. a compiler) during the execution of the compiler. The user input N is the desired address length of the resulting outputted machine language program. The present invention takes a user input N, the address length, and then generates a machine language program from the source program which utilizes N-bit addressing. The cited reference only refers to a hardware implementation in which the address size can be determined at the design stage of the microprocessor, but is then fixed. The reference does not teach having a user input for a compiler to specify the address length of the outputted machine language program. This element of the claimed invention is not taught by any of the references cited in the Office Actions and, therefore, the Office Action has not established a *prima facie* case of obviousness. As stated in Ex Parte Clapp, 227 U.S.P.Q. 972, 973 (Bd. of App. 1985):

> To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

Furthermore, neither Harmon nor Killian et al. teach an "option direction means for holding a user's direction for an overflow compensation" in combination with a "prohibition means for prohibiting a generation of a compensation instruction by the compensate instruction generating means when the option directing means is storing an indication denoting not to compensate" as claimed in amended Claims 13, 20, and 27. The disclosure of Killian et al. cited by the Office Action in support of the rejection refers to a hardware implementation of an overflow detection/compensation circuit (Cols. 16 and 17). The reference does not teach having a user direction determine whether to prohibit the generation of a compensate instruction. Therefore, the rejection under 35 U.S.C. § 103 should not be upheld, since the combination of Killian et al., Harmon, and Sebesta does not disclose these claimed elements of Applicants' invention. Finally, the argument in the first Office Action that it would be obvious "to supply user specified overflow compensation to make the compiler more automatic" (p. 6) is without support in the prior art and is not directed toward Applicants' invention of reducing program size and execution time by allowing the user to specify whether to compensate or not.

Claim 44 and 47 claim the feature of determining whether to zero or sign extend based on the type of storage register designated. Specifically, zero extension is performed when the immediate data is to be stored in a first register means, and code extension is performed when the immediate data is to be stored in a second register means. Thus, the information designating whether a zero or code extension should be performed is conveyed by the type of storage register designated for storing the data. With the present invention, it is unnecessary to provide any explicit demarcation of whether to zero or code extensions should be applied to the immediate data. This feature is not disclosed in the prior art, nor would it have been obvious and, contrary to the Office Action's conclusion, these elements are stated in the claims. See for example, Claim 44, lines 11-22 or Claim 47, lines 16-24. Applicants respectfully request the rejections be reconsidered in light of the above arguments and that the claims be allowed.

Claims 6-12 and 37-43 have been rejected under 35 U.S.C. § 103 as being unpatentable over Harmon and Sebesta as incorporated from the first Office Action. Claims 6-12 should be allowable for at least the reasons stated above. In response to Applicants' arguments in the first Office Action in regard to Claims 37-43, the second Office Action stated "a protocol where the number of bits to be transmitted is designated according to an external indication' is not stated in the claims." However, the Applicants respectfully submit that this feature is stated in the claims as "external-access-width control means" and "external-access executing means" as claimed in Claim 37. The Office Actions have provided no prior art references to support the conclusion that the "external-access-width control means" is obvious. Therefore, Claims 37-43 should be allowed.

With regard to Claims 51-55, Claims 51-53 are method claims relating to the process disclosed by Claims 44-50, and should be allowable for at least the reasons stated above. As to Claims 54 and 55, the limitations on which the Applicants relied in the first Amendment are explicitly stated in the claims, contrary to the Office Action, paragraph 7.6. In Claim 54, the Applicants have claimed "a plurality of flag storing means, each for storing a corresponding flag group" and, therefore, there are a plurality of flag groups. Applicants again contend that the prior art of record does not disclose or suggest the claimed combination, including a plurality

of flag storing means, the flag selecting means, and the branch storing means. Therefore, Claim 54 should be allowed.

Newly-added Claims 58-70 are directed to a computer system incorporating the processor and program converting unit of the present invention. As stated in Claim 58, the bit length of the address bus and other components of a processor are determined based on the address bus width of the memory means. The processor has the minimum hardware necessary to run a program having a user selected program size. This results in reduced chip area and power consumption. Furthermore, as long as the address calculations are performed using N bits, where N is greater than the data width M, there will be no reduction in performance of the processor for any $N > M$ selected by the user. Furthermore, the computer system incorporates the program converting unit of the present invention. The program converting unit includes an input N which the user designates to determine the address length of the output machine language program. Such a computer system is not disclosed by the prior art.

Due to the lengthy and involved arguments stated in the response to the first Office Action in the parent application, the Applicants respectfully request the Examiner to review those arguments in light of the above discussion.

It is respectfully submitted that the case is now in condition for allowance, and an early notification of the same is requested. If the Examiner believes that a telephone interview will help further the prosecution of this case, Applicants respectfully request that the undersigned attorney be contacted at the listed telephone number.

Respectfully submitted,

PRICE, GESS & UBELL

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington DC 20231 on February 15, 1996
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Signature

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